A Novel design of low-power, high speed OTA in 50nm-CMOS technology

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Abstract—This paper presents design steps in detail for Operational Transconductance Amplifier (OTA) design with 50nm-CMOS technology. Novel circuits, design choices, design analysis, and calculations are given to show the circuit topology, transistors’ dimensions, and capacitors’ values. Results obtained illustrate our design’s performance that meets all requirements of high speed, ultra low power, and voltage supply variation up to 40%.

Keywords- OTA, telescopic, Beta-Multiplier Voltage Reference, high speed, low power, voltage supply variation

I. INTRODUCTION

There is actually an increasing demand for high-speed and low-power ADC in various applications, e.g. high data-rate wireless connection in battery-powered devices. As an important block in ADC, the Sample/Hold (S/H) circuit must therefore satisfy these characteristics, especially when it is considered one of the most power hungry blocks in high-speed ADC [1]. In its turn, the S/H circuit is strongly affected by its Operational Transconductance Amplifier (OTA) specifications such as bandwidth, DC gain, linearity, settling behavior and power consumption. Therefore, the OTA design is done carefully to meet the requirements of a high-speed and low-power.

Depends on our prioritized characteristics, we can choose an appropriate topology for our OTA: Telescopic, Folded-cascode, Two-stage or Gain-boosted [2]. The telescopic topology is typically considered having higher frequency capability and consuming less power than other topologies, at the price of limited output swing [3], [4]. The high frequency capability results from its particular pole system and parasitic capacitance at source node. It also consumes less power because it has only one stage/one path between the supply rails [3]. Telescopic topology will be therefore used in our OTA design. Other topologies to design a complete OTA will be analyzed and chosen to meet design requirements of high speed, low power.

This paper presents design steps in detail for OTA design with 50nm-CMOS technology. The rest of this study is organized as follows. Section II presents the architecture design that chooses appropriate topologies to meet requirements. Design, calculation in detail is given in section III. Results of our OTA design are shown in next section followed by the section V of conclusion.

II. ARCHITECTURE DESIGN

In this study, due to high speed, low power dissipation requirements and design convenience to meet design specification, two-stage amplifier model is proposed to be used with the first stage providing a high gain and the second, high swings. Our S/H specification design is as follows:

- Voltage supply: 1V ± 40%
- Sampling frequency: 100MHz
- Total error : < 2^-12
- Settling time : < 5ns
- DC Gain : > 500
- Maximum output swing: 2Vp-p
- Feedback capacitor of the SHA: 50fF
- Load capacitance of the SHA: 250fF
- Peak - peak noise : low
- Power dissipation: ultra low power
- CMOS technology: 50 nm

The design choice for 2 stages in our design is presented in following sections.

A. First-Stage Telescopic Amplifier

In the first stage design, a configuration meeting high gain, low power dissipation requirement is focused in design since in this design phase, output swing requirement will be considered in the second stage. Three topologies of telescopic, folded cascode, and current mirror were used in literature. This leads us one concern of which one is suitable in our design. To address this, the comparison between three topologies is presented in Table I.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Telescopic</th>
<th>Folded cascode</th>
<th>Current mirror</th>
</tr>
</thead>
<tbody>
<tr>
<td>High speed</td>
<td>√</td>
<td>√</td>
<td>X</td>
</tr>
<tr>
<td>Low voltage</td>
<td>X</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Low power</td>
<td>√</td>
<td>X</td>
<td>√</td>
</tr>
<tr>
<td>Maximum swing</td>
<td>V_{DD}-5V_{overdrive}</td>
<td>V_{DD}-4V_{overdrive}</td>
<td>V_{DD}-4V_{overdrive}</td>
</tr>
<tr>
<td>Number of pole/Design convenience</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

where V_{DD} is voltage supply, V_{overdrive} = V_{GS}-V_{TH}

From this table, a telescopic is chosen to meet design requirements of high speed, low power. This topology also gives design convenience due to smaller number of pole. Its disadvantage of smaller swing will be solved in the second stage. The telescopic is used in this study as in Fig.1.
In this telescopic topology, all transistors must be biased in saturation area. Particularly, transistors M3-M4, M5-M6 and tail current source M1-M2 are sensitive to the input signals \( v_p \) and \( v_m \), they could be easily outside the saturation area. Therefore, attention on voltage reference design is done to make sure that these transistors M1-M6 are always in saturation. This would insure good common mode rejection, frequency response and gain.

**B. Second-Stage Cascode buffer**

This architecture as in Fig. 2 provides better common mode range, better output swing, as well as the capability of selecting the required overdrive voltage for input transistors to achieve the unity-gain frequency without the output swing limitation. However, its disadvantages are higher input referred noise and higher power dissipation [5] that would be compensated by low power property in first stage of telescopic.

**C. Two-stage Opamp**

As states above, due to high speed, low power dissipation requirements and design convenience to meet design specification, two-stage amplifier model is used by connecting the first stage of telescopic in section A with high gain, low power, high speed and the second stage of cascade buffer in section B with high swings. These two stages are connected via a Miller capacitor as in Fig. 3.

Putting a Miller capacitor between two stages helps to improve circuit stabilization and slew rate.

Stabilization enhancement of using Miller capacitor is due to the fact that the dominant pole is created only by Miller feedback. This insures a high midband gain for the amplifier since the capacitor does not affect the DC response of the amplifier. In this way, the two poles are being split apart and stabilize the feedback amplifiers by greatly narrowing the bandwidth [6]. However, this method of simple pole splitting also gives a right half plane zero which causes negative phase shift, as a result, the little poorer stability [7]. To overcome this issue, MOSFET as nulling resistor is often added. The nulling resistor would be large to obtain no pole splitting [7].

The Miller capacitor also helps to improve the slew rate. Typically, in case of not using Miller capacitor, slew rate would depend on the output capacitor. This means that once we want to increase slew rate, there are two options to choose. Option 1 is increasing the tail current, as a result, increasing the power dissipation. Due to power optimizing, the current must be limited. Option 2 is decreasing the output capacitor. This requires small input capacitor in next stage, as a result difficulty in design. By adding Miller capacitor, the slew rate would not depend on output capacitor, so we could decrease the Miller capacitor to increase slew rate with no need to change current tail, and therefore no change in power dissipation.

**D. Voltage reference**

The objective of voltage reference is to establish a DC voltage that is independent of the supply, process and has a well-defined behavior with temperature. In literature, there are two popular methods to create the voltage reference: band gap voltage reference (BGVR) [2], and Beta-Multiplier Voltage Reference (BMVR) [8]. Considering advantages and disadvantages between them in CMOS process, BMVR is chosen in this study because it offers some important improvements in temperature and process variation over BGVR.

**E. Common Mode Feedback**

Using a feedback in fully-differential amplifier will determine the differential signal voltages, but does not affect the common-mode voltages. Therefore, it’s necessary to add additional circuitry to determine the output common-mode
voltage and to control it to be equal to specified voltage (half of power-supply voltage) that is 500mV in this study. This circuitry is named as the common-mode feedback (CMFB) circuitry. There are different types of CMFB in literature, in this study, Switched-Capacitor CMFB (SC-CMFB) as in Fig. 4 is chosen thank to its properties of no restrictions on the maximum allowable differential input signals, no additional parasitic poles in the CM loop, and high linear [9] and low voltage supply [10].

![Figure 4. Switched capacitor common mode feedback](image)

The transistors and capacitors used for SC-CMFB in this study are as follows: all of transistors have width=0.5 µm, length= 50 nm; C1 =50 fF, C2 = 10 fF

### III. DESIGN AND CALCULATIONS

#### A. Two stage amplifier with cascode output

1) **Design**

The total error is given by

\[
e_{\text{total}} = \frac{1}{A\beta} + e^{-\frac{t_s}{\tau}}
\]

Where: \(A\) is the open loop gain, \(\beta\) is the feedback factor; \(t_s\) and \(\tau\) are determined by the equations as follows:

\[
\tau = \frac{1}{\beta \omega_u} \quad t_s = \frac{t_{\text{sample}}}{2}
\]

For two-stage amplifier, Unity-Gain frequency can be obtained by:

\[
\omega_u = \frac{g_{m1}}{c_2}
\]

Settling time is dominated by Slew Rate parameter from equation (4):

\[
SR = \frac{I_{\text{tail}}}{c_2}
\]

where \(c_2\) is Miller capacitor in Fig.1 and Fig. 3.

Due to sampling frequency requirement of 100MHz (means 5ns per sample), \(I_{\text{tail}}=26\mu A\) is chosen for low power dissipation, and \(C_1=C_2=C_c=50\text{fF}\).

Technology in this design is 50nm, short-channel model is used, and as a result, the equation of \(I_d\) in each MOSFET is determined by:

\[
I_D = V_{\text{sat}} C_{\text{ox}} \frac{W}{L} (V_{gs} - V_{TH} - V_{DS, sat})
\]

And transconductance is given by:

\[
g_m = V_{\text{sat}} C_{\text{ox}} \frac{W}{L}
\]

For high-speed design, channel length L should be equal to feature size of 50nm. However, using channel length as a feature size results in large mismatches between devices and low MOSFET output resistance [11]. As a result, noise at the differential input occurs.

For general analog design, the overdrive voltage could be set to 5\% of VDD. For high-speed design, we might set the overdrive voltage to 10\% of VDD or higher [11].

The size of NMOS is chosen 0.5µ/50n to meet the requirement of Drain current value. To match the current driver, the size of 1µ/50n is chosen for PMOS. These ratios ensure that NMOS and PMOS have the same Gate-Source voltage, which facilitates the bias circuit design.

With an overdrive voltage of 100 mV (10\% Vdd), the threshold voltages will be 280 mV. The value of Gate-Source voltage is determined using simulation tool in order to attain the desired slew rate. With 13µA of \(I_{\text{DS}}\), simulation tool give us 400mV of Gate-Source voltage.

Thermal noise must be taken into account in this low-noise design. Thanks to the capacitor selecting guide from [12], we can choose the value of capacitor to satisfy the noise requirement. In this design, a load capacitance of 250 fF for a peak-to-peak noise of 750 \(\mu\text{V}\) is used.

The following table shows the transistor dimensions and capacitor value used in this design.

<table>
<thead>
<tr>
<th>Transistor Dimensions and Capacitor in Telescopic</th>
<th>Width(µm)</th>
<th>Length(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1/M2</td>
<td>0.5</td>
<td>50</td>
</tr>
<tr>
<td>M3/M4</td>
<td>0.5</td>
<td>50</td>
</tr>
<tr>
<td>M5/M6</td>
<td>0.5</td>
<td>50</td>
</tr>
<tr>
<td>M7/M8</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>M9/M10</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>M11/M12</td>
<td>0.5</td>
<td>50</td>
</tr>
<tr>
<td>M13/M14</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>Capacitor Value (fF)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{\text{Miller}})</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>(C_{\text{load}})</td>
<td>250</td>
<td></td>
</tr>
</tbody>
</table>

2) **Enhancing design of output buffer**

In differential amplifier, Common Mode Feedback (CMFB) circuit is required to obtain a desired common mode output value.

With CMFB added to the circuit, we assume that the output value of diff-amp \(V_{\text{bias}}\) is 600 mV because we want to use the voltage at the first stage to bias the second stage. Followed by this assumption, the drain current in all MOSFETs will be 20\(\mu\text{A}\) and the gate potentials of the NMOSs \(V_{\text{bias}}\) will be 400 mV.

Because of the symmetry of the circuit as in Fig. 2, the output is also at 400 mV. This mean the output will swing roughly around 400mV while the expected value at output is typically 500mV. In order to increase the output voltage to 500 mV, we must decrease the potential on the PMOS gates until the output swing attain 500 mV. Solution to this issue is shown in Fig. 5 as half circuit of circuit in Fig. 2. One NMOS M14 is added to cascode the output buffer’s NMOS. This adding allows the amplifier's output to swing more freely [11], while the speed wouldn't be affected. Besides, this configuration also increases the amplifier gain which helps to decrease total error in S/H design and increase resolution in ADC design.
The dimensions of MOSFETs in output buffer stage (Fig. 2 and Fig. 5) are shown in Table III.

### Table III. Transistor Dimensions in Output Buffer Stage

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width(µm)</th>
<th>Length(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{27}/M_{26}$</td>
<td>0.5</td>
<td>50</td>
</tr>
<tr>
<td>$M_{25}/M_{24}$</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>$M_{23}/M_{22}$</td>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>$M_{21}/M_{20}$</td>
<td>4</td>
<td>50</td>
</tr>
</tbody>
</table>

#### B. Voltage Reference

1) Design

The basic Beta-Multiplier Voltage Reference as in Fig. 6 is chosen to start the design. After considering design and its properties, our proposed BMVT circuit is given in next section.

![Figure 6. Basic Beta-Multiplier Voltage Reference circuit](image)

For short channel process in BMVR circuit, $I_D$ is given as:

$$I_D = I_{REF} = V_{sat}C_{ox}(V_{GS} - V_{TH} - V_{DS,sat})$$  

(7)

$V_{REF}$ for BMVR of short-channel is:

$$V_{REF} = V_{GS2} + I_{REF}R$$

(8)

where $V_{GS2} = \frac{L_{m,REF}}{V_{sat}C_{ox}W} + V_{TH} + V_{DS,sat}$ and

$$V_{REF} = \frac{L_{m,REF}}{V_{sat}C_{ox}W} + V_{TH} + V_{DS,sat}$$

From (7), (8), the resistance can be obtained:

$$R = \frac{1}{g_m}(1 - \frac{1}{k})$$

(9)

where $M_{24} = k. M_{23}$

In design, it’s important to get condition of $V_{REF}=V_{GS24}$ as a result $I_{REF}=0$. This means that $I_{REF}$ would be independent of $R$. Therefore, one good point could be extracted is that dependency of $V_{REF}$ on temperature coefficient in resistance is very small.

In this design, the transistor dimensions are chosen as in Table IV. The result of $V_{bias_n}$ is 400mV that meets bias voltage requirement for NMOS in section III.A.1.

### Table IV. Transistor Dimensions for Basic BMVR Circuit

<table>
<thead>
<tr>
<th>Device</th>
<th>Width(µm)</th>
<th>Length(nm)</th>
<th>Resistance (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{23}$</td>
<td>0.5</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>$M_{24}$</td>
<td>2</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>$M_{25}/M_{26}$</td>
<td>0.5</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>$M_{21}/M_{22}$</td>
<td>1</td>
<td>50</td>
<td></td>
</tr>
</tbody>
</table>

2) Enhancing power supply sensitivity

To decrease the power supply sensitivity, the change of $V_{DS24}$ due to $V_{DD}$ variation should be reduced as small as possible. One solution for this issue is proposed in Fig. 7 by adding a differential amplifier to the BMVR circuit. The idea of this approach is using amplifier to compare and regulate the voltage of $M_{23}$’s drain to be equal with the voltage of $M_{24}$’s drain. Adding the amplifier also results the increased output resistance that help to obtain good operation in larger voltage supply variation.

![Figure 7. Proposed BMVR circuit for the short channel MOSFET](image)

However, BMVR circuit in Fig. 7 has two operating points because of a positive feedback, so the initial state should be determined by the start-up circuit shown in Fig. 8 [13].

![Figure 8. Start-up circuit for BMVR circuit](image)
All devices’ sizes are shown in Table V.

### Table V. Transistor dimensions for BMVR and start-up circuits

<table>
<thead>
<tr>
<th>Device</th>
<th>Width[μm]</th>
<th>Length[mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>M23</td>
<td>0.5</td>
<td>50</td>
</tr>
<tr>
<td>M24</td>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>M25/M26</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>M27/M28</td>
<td>0.5</td>
<td>100</td>
</tr>
<tr>
<td>M29/M30</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>M21/M22</td>
<td>0.5</td>
<td>50</td>
</tr>
</tbody>
</table>

IV. Result

Simulation results of our design is determined at typical temperature and done by Spice. Frequency analysis of the OTA is shown in Fig. 9.

![Figure 9. Frequency response of our OTA](image)

Bode plot obtained as in Fig. 9 shows that DC gain is 57.15 dB, Unity Gain of 604.7 MHz with 250F load capacitance. Phase margin (PM) achieved with this load is 65.35°.

The whole performance of our design and comparison with previous works are presented in Table VI.

### Table VI. Performance of OTAs

<table>
<thead>
<tr>
<th>Main Characteristics</th>
<th>This work</th>
<th>[5]</th>
<th>[14]</th>
<th>[15]</th>
<th>[16]</th>
<th>[17]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply (V)</td>
<td>1</td>
<td>3.3</td>
<td>1.8</td>
<td>2.5</td>
<td>3.0</td>
<td>3.3</td>
</tr>
<tr>
<td>DC Gain (dB)</td>
<td>57.15</td>
<td>91.7</td>
<td>90.39</td>
<td>102</td>
<td>95</td>
<td>95</td>
</tr>
<tr>
<td>Unity gain (MHz)</td>
<td>604.7</td>
<td>-</td>
<td>700.7</td>
<td>822</td>
<td>412</td>
<td>500</td>
</tr>
<tr>
<td>Phase margin (Degree)</td>
<td>65.35</td>
<td>-</td>
<td>63.85</td>
<td>62.5</td>
<td>75</td>
<td>55</td>
</tr>
<tr>
<td>Input common mode range (V)</td>
<td>499-501</td>
<td>-</td>
<td>0.5</td>
<td>1.2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Output swing (V)</td>
<td>0.3-1</td>
<td>-</td>
<td>0.5</td>
<td>1.2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>0.56</td>
<td>-</td>
<td>3.24</td>
<td>35</td>
<td>12.8</td>
<td>14.5</td>
</tr>
<tr>
<td>Settling time (ns)</td>
<td>2.05</td>
<td>5.3</td>
<td>2</td>
<td>3.5</td>
<td>7.5</td>
<td>-</td>
</tr>
<tr>
<td>Load capacitance (pf)</td>
<td>0.25</td>
<td>0.5</td>
<td>4</td>
<td>1.9</td>
<td>0.5</td>
<td>-</td>
</tr>
<tr>
<td>Voltage supply variation (%)</td>
<td>40%</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

The performance of design shows that the design satisfies the requirement. The DC gain in this study of 57.15dB is relatively low for some applications, but our design gives low power, high speed as a trade-off, and could be used with voltage supply variation up to 40%. This good result in voltage supply variation is obtained thank to proposed BMVR in Fig. 7.

V. Conclusion

This paper presents design steps in detail for OTA design with 50nm-CMOS technology. Novel circuits, design choices, design analysis, and calculations are given to show the circuit topology, transistors’ dimensions, and capacitors’ values. Results obtained illustrate our design’s performance that meets all requirements of high speed, ultra low power, and voltage supply variation up to 40%.

### Reference