Abstract—The synchronized oscillator composed of the plural CMOS ring oscillators is interesting for improving the performances of the oscillators. Several different circuits using the CMOS ring oscillators are discussed in this report. These are the tetrahedral oscillator, ORIGAMI oscillator, precise delay generator, braided connected oscillator, and the newly proposed oscillator embedded the pincer movement operation. These oscillators are applicable to different kind of applications. The oscillator embedded the pincer movement operation is simulated to show the performance, where 0.18μmCMOS process models are used.

I. INTRODUCTION

CMOS ring oscillators are used for the clock recovery circuits, the delay time signal generation circuits, frequency reference circuits, and the quadrature signal generation, etc.. The prospective roles of the synchronized oscillator are the quadrature signal generation, and the precise delay signal generation [1].

In these applications, the phase noise and jitters specifications are important. In the quadrature signal generation circuit, the phase accuracy of 90° is also important. It is well known that the ring oscillator is inferior to the LC tank oscillator in these specifications, the ring oscillator leaves much room for improvement.

The ORIGAMI oscillator [2] for quadrature signal generation was introduced recently. The circuit schematics was based on the Nauta’s OTA in 1992 [3], which is applied to the transconductance-C filters. In 1996, without changes to the circuit topology, a tetrahedral oscillator [4] was reported. The tetrahedral oscillator can be categorized as a ring oscillator with hysteresis delay, and its oscillation mechanism is analyzed in [5]. In 2002, the circuit was used to realize a CMOS VCO [6]. The ORIGAMI oscillator was created by modifying the circuit schematic of the tetrahedral oscillator, and has different characteristics from the tetrahedral oscillator.

For the precise delay signal generation circuit, the oscillator array using CMOS ring oscillators was proposed to generate precise delay time in 1993 [1]. The precise delay time signal generation scheme is important, because the minimum time scale of the delay time signal created by the CMOS ring oscillator is normally determined by the delay time of the CMOS inverter composed of the CMOS ring oscillator. To obtain finer time scale, each oscillator oscillation waveform is slightly shifted by using the oscillator array configuration. The quantity of the phase shift is defined by the number of the array elements, where each array element is composed of the CMOS ring oscillator. Connections or couplings between the array elements are realized by the wired OR configuration [1]. In 2011, the oscillator array with the braided connections is proposed to improve the oscillator phase noise and jitters performance [7]. The coupling between array elements of the proposed oscillator array show the bidirectional and tight connections property.

To improve the phase noise performance of the oscillator array with the braided connections, the modified topology of the oscillator array is newly proposed in this paper, where each array element waveform is dominated by the waveform of the adjacent upper and lower array elements.

In Sec.2, several different circuit topology are compared with each other. In Sec.3, the newly proposed oscillator array is described. In Sec.4, the performance comparison is also reported. 0.18μm CMOS process models and SPECTRE phase noise simulation are used for the performance verification and comparisons.

II. CONVENTIONAL SYNCHRONIZED OSCILLATOR COMPOSED OF THE PLURAL CMOS RING OSCILLATORS

A. Naua’s OTA and Tetrahedral oscillator

Figure 1(a) shows the Nauta’s OTA [3] and Fig.1(b) is the application to the quadrature oscillator [6]. The oscillation mechanism of the circuit in Fig.1(b) is explained by the function of the ring oscillator with hysteresis delay cells [5].

The tetrahedral oscillator [4] shown in Fig. 2 generates a quadrature signal by using four three-stage ring oscillators that overlap each other, and it is designed to generate high-frequency signals for clock-recovery circuits and other such applications. Note that the circuit topology in Fig.1(b) is the same as the topology in Fig.2.

B. ORIGAMI oscillator

Imitating the techniques of the traditional Japanese art of origami, the tetrahedral oscillator is constructed as shown in Fig. 3. In Fig. 3(a), the three-stage ring oscillators in the folds are unfolded, generating the circuit in Fig. 3(b). The circuit shown in Fig. 3(b) is further modified by merging the redundant adjacent inverters with each other, and the circuit
Fig. 1. (a) Nauta’s OTA, (b) Quadrature oscillator using the Nauta’s OTA.

Fig. 2. Tetrahedral oscillator [4], in which \( k < 1 \) is the size of the inverter [4].

in Fig. 3(c) is developed. The circuit in Fig. 3(c) is called an ORIGAMI oscillator\(^1\).

To formulate the mechanism of the quadrature signal generation of the ORIGAMI oscillator, an alternative circuit schematic of the ORIGAMI oscillator is shown in Fig. 4. In this figure, the ORIGAMI oscillator is divided into four individual oscillators. Each individual oscillator has the same schematic, and is composed of two three-stage CMOS inverter ring oscillators, where one CMOS inverter is commonly used.

The ORIGAMI oscillator is characterized by

1) Number of the individual oscillator, \( M \), is 1,2,3,\ldots.
2) Oscillation frequency, \( \omega_0 \) is the same as the oscillation frequency of the 3-stage CMOS ring oscillator.
3) Oscillation frequency, \( \omega_0 \) is independent from the number, \( M \).

Especially, 3) is the specific feature of ORIGAMI. The minimum delay time, \( \Delta \tau \) generated by ORIGAMI is formulated as:

\[
\Delta \tau = \frac{6}{M} \tau_D
\]  

, where \( \tau_D = \frac{\pi}{3 \omega_0} \) is the delay time of CMOS inverter gate.

C. Ring oscillator Array

The oscillator array in [1] is shown in Fig. 5. \( M \) \( N \)-stage CMOS ring oscillators are piled up as shown in Fig. 5. \( (i) \)-th CMOS ring oscillator’s \( (j) \)-th node signal is transferred through CMOS inverter to \( (i+1) \)-th CMOS ring oscillator’s \( (j+1) \)-th node, where \( i \) and \( j \) are \( i = 1,2,\ldots,M \), \( j = 1,2,\ldots,N \). To generate precise delay time, the bottom array element node \( B_i \) is fed-back to the top array element node \( R_{i+k} \) in [1], where \( k = 0, \pm 2, \cdots \). The minimum delay time generated by the conventional CMOS ring oscillator is \( \tau_D \), and \( \Delta \tau \) is the precise delay time generated by the array oscillator.

\(^1\)The name ORIGAMI was applied by Dr. Chris Mangelsdolf, Analog Devices, Inc.
Fig. 4. Alternative circuit schematic of the ORIGAMI oscillator. The ORIGAMI oscillator is a four-stage ring oscillator composed of 4 individual oscillators.

Fig. 5. Conventional CMOS ring oscillator array for precise delay generation, where $N = M = 3$ [1].

are formulated as follows [1]:

$$\Delta \tau = \frac{2N}{M} \tau_D$$  \hspace{1cm} (2)

D. Ring oscillator Array with Braided connection

Figure 6 shows the example circuit of the oscillator array with braided connections. The circuit is introduced to improve the phase noise performance of the oscillator.

Fig. 6. Ring oscillator array with Braided connection.

III. OSCILLATOR ARRAY EMBEDDED THE PINCER MOVEMENT OPERATION

The phase noise performance improvement of the oscillator array with braided connections is obtained when the coupling between the ring oscillators is strong [7]. Note that “the coupling is strong” means that the gain of the inverter used for the coupling is higher than the gain of the inverter composed of the CMOS ring oscillator. This result suggests tight coupling is required for the phase noise performance improvement.

Figure 8 shows the newly proposed oscillator array, where the same labeled wires are connected each other. For example, the wires labeled “a” are connected with each other. The oscillator array shown in Fig.8 is composed of $MN$-stage CMOS ring oscillators. Each $N$-stage CMOS ring oscillator is denoted by the dashed line box named $\beta$.

The dotted line box $\alpha$, which is named Pincer Drive Block, PDB, is the key element of the proposed circuit, where the key element is composed of three inverters.

Three input signals of PDB are the waveform of three adjacent ring oscillators. Normally, the oscillation waveform of all ring oscillators are synchronized with each other. On the condition that the node waveform is contaminated by the noise, the device mismatch, etc., the expected rising or falling time is slightly shifted as shown in Fig.9. In this figure, if PDB is used, the undesired rising or falling time shift quantity is relaxed.

IV. SIMULATED RESULTS

To verify the performance of the proposed ring oscillator array, the phase noise performance are simulated using SPECTRE. The channel length of all transistors is 0.18$\mu$m, Level 3 MOSFET model, 1/f noise parameters are $a_f = 1.0$, $k_f = 2.6 \times 10^{-26}$ for pMOS, and $k_f = 2.5 \times 10^{-28}$ for nMOS are assumed. The channel widths of each inverter are $W=1\mu$m for nMOS, $W=2\mu$m for pMOS, respectively.
Fig. 8. Proposed oscillator array, where $M = N = 3$.

In Fig. 10, phase noise simulated at $\Delta f = 1$ MHz is shown. When $M$ increases, the phase noise is improved. When $N$ is changed from 3 to 5 or 7, the phase noise is improved about 7.6 dB or about 12 dB, respectively.

The performance is also checked by the following FOM [8]:

$$\text{FOM}_{VCO} = \left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L(\Delta f)} P$$  \hspace{1cm} (3)

where $f_0$ is the oscillation frequency, $L(\Delta f)$ is the noise spectrum density detuning $\Delta f$ from $f_0$, and $P$ is the dissipation power.

Table I shows the simulated oscillation frequency, power dissipation, and FOM.

V. CONCLUSION

In this paper, several different oscillator topology are reviewed. Then, the CMOS ring oscillator array embedded the pincer movement operation is newly introduced. The phase noise performance of the proposed oscillator array can be improved if the stage of the ring oscillator is increased, and the number of the ring oscillators.

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